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15/1 AP
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Jack C. Wybenga, et al.
Serial No. : 10/658,977
Filed : September 10, 2003
For : APPARATUS AND METHOD FOR PERFORMING HIGH-SPEED
LOOKUPS IN A ROUTING TABLE
Group No. : 2189
Examiner : Reginald Glenwood Bragdon

MAIL STOP APPEAL BRIEF - PATENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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Date: May 12, 2008

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FEE TRANSMITTAL

For FY 2008

 Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$)

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Complete if Known

Application Number	10/658,977
Filing Date	September 10, 2003
First Named Inventor	Jack C. Wybenga
Examiner Name	Reginald Glenwood Bragdon
Art Unit	2189
Attorney Docket No.	2003.09.014.BNO

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION
1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity	Fee (\$)	Small Entity	Fee (\$)	Small Entity	
Utility	310	155	510	255	210	105	
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES
Fee Description

Each claim over 20 (including Reissues)

Fee (\$)	Small Entity
50	25
210	105
370	185

Each independent claim over 3 (including Reissues)

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims
- 20 or HP =	x	=		Fee (\$)

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	
- 3 or HP =	x	=		Fee (\$)

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 =	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): Appeal Brief

Fees Paid (\$)

\$510.00

SUBMITTED BY

Signature	<i>John T. Mockler</i>	Registration No. (Attorney/Agent) 39,775	Telephone 972-628-3600
Name (Print/Type)	John T. Mockler		Date May 12, 2008

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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APPEAL BRIEF

Sir:

Applicants herewith respectfully submit that the Examiner's decision of September 17, 2007, finally rejecting Claims 1-22 in the present application, should be reversed, in view of the following arguments and authorities. This Brief is submitted in response to the Notice of Panel Decision mailed April 11, 2008. A check in the amount of \$510.00 is enclosed for the fee of filing a Brief on Appeal, but please charge any additional necessary fees to Deposit Account No. 50-0208.

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TABLE OF CONTENTS

Table of Authorities	3
Real Party in Interest	4
Related Appeals or Interferences	5
Status of Claims	6
Status of Amendments after Final.....	7
In General.....	8
Support for Independent Claims	8
Grounds of Rejection to be Reviewed on Appeal.....	11
1. Are Claims 1-22 anticipated under 35 U.S.C. § 102(b) by U. S. Patent No. 6,192,051 to Lipman <i>et al.</i> (“Lipman”)?.....	11
ARGUMENT	12
Stated Grounds of Rejection	12
Legal Standards.....	13
Analysis of Examiner's Rejection	13
First Ground of Rejection	14
Grouping of Claims.....	35
REQUESTED RELIEF	36

APPENDIX A - Text of Claims on Appeal

APPENDIX B - Copy of Formal Drawings

APPENDIX C - Evidence Appendix

APPENDIX D - Related Proceedings Appendix

Table of Authorities

Cases

<i>In re Bond</i> , 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990)	13
<i>In re Donohue</i> , 766 F.2d 531, 226 U.S.P.Q. 619 (Fed. Cir. 1985)	13

Regulations

MPEP § 2131	13
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Real Party in Interest

The real party in interest, and assignee of this case, is Samsung Electronics Co., Limited.

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

**ATTORNEY DOCKET NO. 2003.09.014.BN0
U.S. SERIAL NO. 10/658,977
PATENT**

Status of Claims

Claims 1-22 are under final rejection, and are each appealed.

ATTORNEY DOCKET No. 2003.09.014.BN0
U.S. SERIAL NO. 10/658,977
PATENT

Status of Amendments after Final

No claims were amended after final rejection.

Summary of Claimed Subject Matter

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

In General

The present application is directed, in general, to massively parallel routers and, more specifically, to a massively parallel, distributed architecture router that contains a routing (or forwarding) lookup mechanism capable of performing high-speed lookups. *Page 1, lines 6-10.*

Support for Independent Claims

Note that, per 37 CFR §41.37, only each of the independent claims are discussed in this section, as well as any claims including means-plus-function language that is argued separately below. In the arguments below, however, the dependent claims are also discussed and distinguished from the prior art. The discussion of the claims is for illustrative purposes, and is not intended to effect the scope of the claims.

Claim 1 describes, for use in a router (e.g., 100), a lookup circuit (e.g., 300) for translating received addresses into destination addresses. The circuit includes M pipelined memory circuits (e.g., 322, 323, 324, 325) for storing a trie table capable of translating a first received address into a first destination address. The M memory circuits are pipelined such that a first portion of the first received address accesses an address table in a first memory circuit (e.g., *from 321 to a table in 322*)

and an output of the first memory circuit accesses an address table in a second memory circuit (e.g., *from a table in 322 to a table in 323*). (Application, Page 4, Line 19 – Page 6, line 17; Page 9, Lines 9 – Page 14, Line 8; and Figures 1-3).

Claim 11 describes a router (e.g., 100) for interconnecting N interfacing peripheral devices. The router includes a switch fabric (e.g., 155a and 155b) and a plurality of routing nodes (e.g. *routing nodes 110, 120, 130, and 140*) coupled to the switch fabric. Each of the routing nodes includes a plurality of physical medium device (PMD) modules (e.g., *PMD-a and PMD-b*) capable of transmitting data packets to and receiving data packets from selected ones of the N interfacing peripheral devices. Each of the routing nodes also includes an input-output processing (IOP) module (e.g., *IOP 116, 126, 136, 146*) coupled to the PMD modules and the switch fabric and capable of routing the data packets between the PMD modules and the switch fabric and between the PMD modules. Each of the routing nodes also includes a lookup circuit (e.g., 300) associated with the IOP module for translating received addresses associated with the data packets into destination addresses, the lookup circuit comprising M pipelined memory circuits (e.g., 322, 323, 324, 325) for storing a trie table capable of translating a first received address into a first destination address, wherein the M memory circuits are pipelined such that a first portion of the first received address accesses an address table in a first memory circuit (e.g., *from 321 to a table in 322*) and an output of the first memory circuit accesses an address table in a second memory circuit (e.g., *from a table in 322 to a table in 323*). (Application, Page 4, Line 19 – Page 6, line 17; Page 9, Lines 9 – Page 14, Line 8; and Figures 1-3).

Claim 21 describes a method for translating a first received address into a first destination address using M pipelined memory circuits (e.g., 322, 323, 324, 325) that store a trie table. The method includes accessing an address table in a first memory circuit using a first portion of the first received address (e.g., *from 321 to a table in 322*). The method also includes outputting from the address table in the first memory circuit a first address pointer that indexes a start of an address table in a second memory circuit (e.g., *from a table in 322 to a table in 323*). The method also includes accessing the address table in the second memory circuit using the first address pointer and a second portion of the first received address. (*Application, Page 4, Lines 3 – 10 ; Page 10, Line 8 – Page 14, Line 14; and Figures 2 and 3*).

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-22 anticipated under 35 U.S.C. § 102(b) by U. S. Patent No. 6,192,051 to *Lipman et al.* (“Lipman”)?

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

1. In the September 17, 2007 Office Action, Claims 1-22 were rejected under 35 U.S.C. § 102(b) as anticipated by *Lipman al.* (“*Lipman*”).

Legal Standards

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. (MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)).

Analysis of Examiner's Rejection

All claims are rejected as anticipated by Lipman. Lipman has some similarity to some claim features, but does not teach the claimed inventions identically, as required by an anticipation rejection.

First Ground of Rejection

Claims 1-22 were rejected under 35 U.S.C. § 102(b) as anticipated by *Lipman al.* (“*Lipman*”).

Claim 1

Independent claim 1 describes

For use in a router, a lookup circuit for translating received addresses into destination addresses comprising:

M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

Independent claim 1 requires “a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit”. This feature is not taught or suggested by Lipman.

While Lipman’s Figure 11 does show that IP address bits [31:16] provide the index of an entry in the level-1 tree 150 (col. 15, lines 59-61), the output “Next Tree Index” (the “NT pointer”) is not used to “access[] an address table in a second memory circuit” where the second memory circuit

is one of the “M pipelined memory circuits”, as claimed in Claim 1. Instead, the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

For the convenience of the Board, Lipman's Figure 11 is reproduced below:

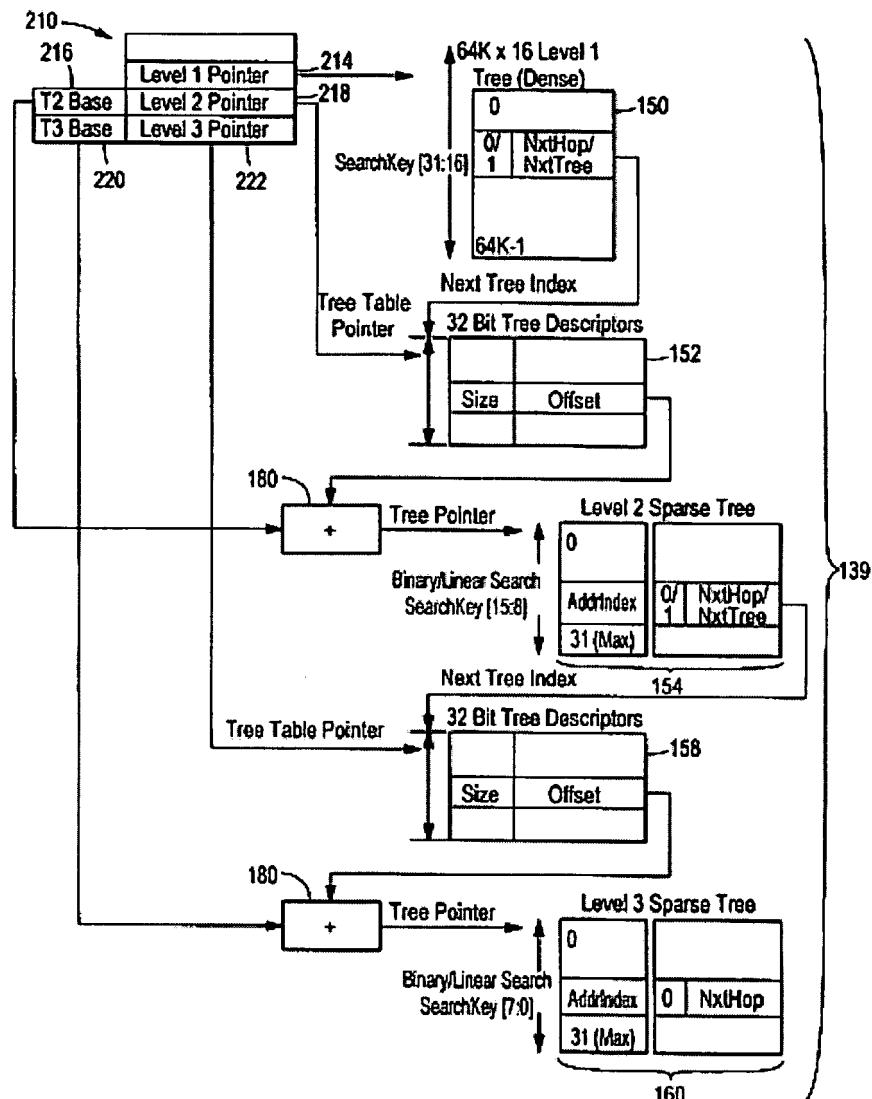


FIG. 11

Figure 11 shows that the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67), and nothing teaches or suggests that the forwarding table is a pipelined memory circuit, as required by the claim. That is,

rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

The Examiner now indicates that he believes that element 144 portion “128.63” satisfies the claimed “first portion of said first received address”. On the contrary, Lipman describes that “A portion of the level 1 tree 140 is shown in FIG. 7, including locations 128.63 through 128.68.” *Col. 10, lines 59-60.* Applicant assumes that this is a typographic error in the patent, and the reference to “140” should be to “144”. Note that this refers to Lipman’s Figure 7, not Figure 11, upon which the bulk of the Examiner’s analysis relies.

The Examiner also indicates that Lipman’s next tree table 152 is the claimed “address table in the second memory circuit”. Of course, by combining element 144 from Figure 7 and element 152 of Figure 11, the Examiner is unable to show at all that there are any pipelined memory circuits, as these two figures do not show any common elements interrelating. Figure 11 is describing a compressed tree, Figure 7 is describing an uncompressed tree, and these do not interrelate.

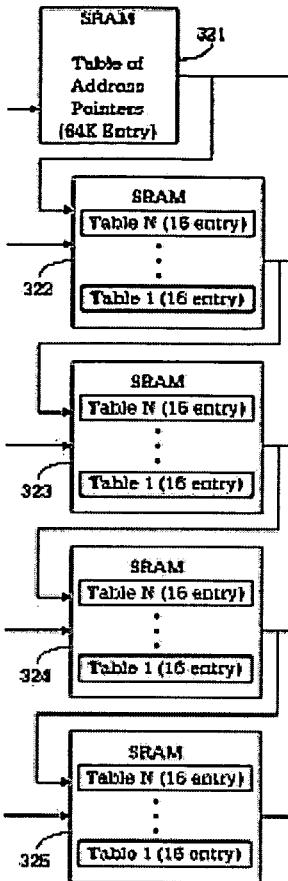
The Examiner now responds with a broad interpretation of “memory circuit” that describes “a combination of interconnected electrical components or pathways that perform a specific task, that being data storage”, and indicates that these are shown in Figure 8. Figure 8 shows a data structure, by Lipman’s own description, not any interconnected electrical components or pathways

corresponding to the Examiner's own definition. Figure 7 is also a data structure. Data structures are not memory circuits.

Certainly a data structure is stored in a physical memory comprising memory circuits. However, a typical physical memory is not comprised of pipelined memory circuits, and certainly not in the manner claimed. Nothing in Lipman describes pipelined memory circuits as claimed.

In fact, though Lipman shows multiple tables that point to each other, nothing in Lipman's description teaches or suggests a lookup circuit comprising "M pipelined memory circuits" as claimed. The Examiner's statement that "these memory circuits are 'pipelined' in that they each point to another circuit" is not persuasive. Those of skill in the art recognize that a "pipeline" is a series of elements each connected so that the output of one element is an input of the next element. See, for example, Figure 3 of the present application, reproduced below, where the output of each pipelined SRAM is an input to the next one in series. Lipman does not appear to teach or suggest such a pipeline at all, much less pipelined memory circuits.

A portion of Figure 3 of the instant application is reproduced below. Note that SRAM 321 is pipelined with 322, 323, 324, and 325, in that each memory circuit has an output connected to the input of the next memory circuit.



The Examiner refers to Lipman's Figure 7 for "pipelined memory circuits", but this figure shows a diagram of a data structure, not memory circuits. If the Examiner is intending to imply that the actual semiconductor circuits that comprise each bit/cell of a memory are the "memory circuits", then the Examiner will surely recognize that these are not typically pipelined, and Lipman certainly doesn't teach any such pipelining. Lipman doesn't teach series connections or pipelining of memory circuits at all.

The Examiner responds that "Lipman teaches pipelining via the levels of the 'tree' that are accessed in sequence. For example, a first tree level is accessed, followed by a second level, and

third (i.e. a pipeline).” The Examiner’s response illustrates his misunderstanding. The sort of sequential access described by the Examiner is not a pipeline, as recognized by those of skill in the art. In a pipeline, data passes from a first element, directly to the next element, and then directly to the element after that. This is very different from, for example, a processor that sends data to/from a first element, then sends data to/from a second element, then sends data to/from a third element. A pipeline of elements is connected in series, not merely accessed in sequence.

The Examiner’s statement that “Pipelining is a term which is used to identify strings of several data or objects” is simply incorrect, particularly as applied to “strings of data”. The Examiner was requested to cite the source of this remarkable definition, but failed to do so.

In the Advisory Action, the Examiner makes the statement that “Pointers are used as simply [sic] representations of elements within circuits that are themselves inputs to another element.” Applicant respectfully notes that the Examiner may not fully understand the difference between a data structure and a physical hardware circuit – a pointer in a data structure normally has no relation at all to the underlying hardware, and nothing in Lipman suggests that it does so in this case.

The rejections should be reversed.

Claims 2 and 12

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the output of the first memory circuit comprises a first address

pointer that indexes a start of the address table in the second memory circuit. This is not taught by Lipman.

The Examiner is able to show a data structure with a pointer to an address table. However, this does not meet the claim limitation, which requires an output of a first memory circuit having a first address pointer that indexes a start of the address table in the second memory circuit, where the first and second memory circuits are pipelined, as required by the parent claim. Again the Examiner attempts to inappropriately mix Lipman's Figs. 7 and 11.

As described above, the output of the level-1 tree 150 (the NT pointer) is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). Lipman also describes that the base of the level-2 next tree table 152 is pointed to by the level 2 pointer 218 from the level pointer block 210. As such, it is clear that the NT pointer does not index a start of the address table in the second memory circuit, as claimed.

These rejections should be reversed.

Claims 3 and 13

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the the first address pointer and a second portion of the first received address access the address table in the second memory circuit. This is not taught by Lipman.

The Examiner is able to show a pointer to an address table. However, this does not meet the claim limitation, which requires the first address pointer be an output of a first memory circuit, where the first and second memory circuits are pipelined, as required by the parent claim.

These rejections should be reversed.

Claims 4 and 14

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that an output of the second memory circuit accesses an address table in a third memory circuit. This is not taught by Lipman.

Element 154, referenced by the Examiner, is not an output of a second memory circuit, where the second and third memory circuits are pipelined, as required by the parent claim.

These rejections should be reversed.

Claims 5 and 15

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that output of the second memory circuit comprises a second address pointer that indexes a start of the address table in the third memory circuit. This is not taught by Lipman.

Element 154, referenced by the Examiner, is not an output of a second memory circuit, where the second and third memory circuits are pipelined, as required by the parent claim.

These rejections should be reversed.

Claims 6 and 16

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the second address pointer and a third portion of the first received address access the address table in the third memory circuit. This is not taught by Lipman.

Lipman's Level 3 Sparse Tree is not a third memory circuit, where the first, second, and third memory circuits are pipelined, as required by the parent claim.

These rejections should be reversed.

Claims 7 and 17

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the address pointers output from the M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, the routing table comprising a plurality of destination addresses associated with the received addresses. This is not taught by

Lipman.

There is no such final memory circuit storing a routing table in Figure 11, and the Examiner again inappropriately alleges that Figs. 7 and 11 can be combined somehow to meet the claim limitations, which is unsupported in Lipman, and erroneous in an anticipation rejection.

These rejections should be reversed.

Claims 8 and 18

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require a memory interface capable of selectively applying to the final memory circuit an address pointer associated with the first received address and an address pointer associated with a subsequently received address, such that the address pointer associated with the first received address is applied to the final memory circuit prior to the address pointer associated with the subsequently received address. This is not taught by Lipman.

There is no such final memory circuit storing a routing table in Figure 11, and the Examiner again inappropriately alleges that Figs. 7 and 11 can be combined somehow to meet the claim limitations, which is unsupported in Lipman, and erroneous in an anticipation rejection.

The Examiner also refers to Lipman's Figs. 12-14, which are flow diagrams for creating compressed trees, and have nothing at all to do with the claim limitations. Lipman does not discuss a process as claimed regarding the application of first and subsequent received addresses.

These rejections should be reversed.

Claims 9 and 19

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the M pipelined memory circuits comprise static random access memory (SRAM) circuits. This is not taught by Lipman.

Lipman does not teach, suggest, or even mention SRAM circuits. The Examiner suggests a substitution, which would arguably be appropriate for an obviousness rejection, but certainly is not for an anticipation rejection..

These rejections should be reversed.

Claims 10 and 20

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

These claims require that the final memory circuit comprises a dynamic random access memory (DRAM) circuit. This is not taught by Lipman.

Lipman does not teach, suggest, or even mention DRAM circuits. The Examiner suggests a substitution, which would arguably be appropriate for an obviousness rejection, but certainly is not for an anticipation rejection. It certainly is not appropriate in combination with the parent claim,

which requires some SRAM circuits and some DRAM circuits.

These rejections should be reversed.

Claim 11

Independent claim 11 describes

A router for interconnecting N interfacing peripheral devices, said router comprising:

a switch fabric; and

a plurality of routing nodes coupled to said switch fabric, each of said routing nodes comprising:

a plurality of physical medium device (PMD) modules capable of transmitting data packets to and receiving data packets from selected ones of said N interfacing peripheral devices;

an input-output processing (IOP) module coupled to said PMD modules and said switch fabric and capable of routing said data packets between said PMD modules and said switch fabric and between said PMD modules; and

a lookup circuit associated with said IOP module for translating received addresses associated with said data packets into destination addresses, said lookup circuit comprising M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address

accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

Independent claim 11 requires “a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit”. This feature is not taught or suggested by Lipman.

While Lipman’s Figure 11 does show that IP address bits [31:16] provide the index of an entry in the level-1 tree 150 (col. 15, lines 59-61), the output “Next Tree Index” (the “NT pointer”) is not used to “access[] an address table in a second memory circuit” where the second memory circuit is one of the “M pipelined memory circuits”, as claimed in Claim 1. Instead, the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

Figure 11, reproduced above, shows that the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67), and nothing teaches or suggests that the forwarding table is a pipelined memory circuit, as required by the claim. That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding

table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

The Examiner now indicates that he believes that element 144 portion “128.63” satisfies the claimed “first portion of the first received address”. On the contrary, Lipman describes that “A portion of the level 1 tree 140 is shown in FIG. 7, including locations 128.63 through 128.68.” *Col. 10, lines 59-60.* Applicant assumes that this is a typographic error in the patent, and the reference to “140” should be to “144”. Note that this refers to Lipman’s Figure 7, not Figure 11, upon which the bulk of the Examiner’s analysis relies.

The Examiner also indicates that Lipman’s next tree table 152 is the claimed “address table in the second memory circuit”. Of course, by combining element 144 from Figure 7 and element 152 of Figure 11, the Examiner is unable to show at all that there are any pipelined memory circuits, as these two figures do not show any common elements interrelating. Figure 11 is describing a compressed tree, Figure 7 is describing an uncompressed tree, and these do not interrelate.

The Examiner now responds with a broad interpretation of “memory circuit” that describes “a combination of interconnected electrical components or pathways that perform a specific task, that being data storage”, and indicates that these are shown in Figure 8. Figure 8 shows a data structure, by Lipman’s own description, not any interconnected electrical components or pathways corresponding to the Examiner’s own definition. Figure 7 is also a data structure. Data structures are not memory circuits.

Certainly a data structure is stored in a physical memory comprising memory circuits. However, a typical physical memory is not comprised of pipelined memory circuits, and certainly not in the manner claimed. Nothing in Lipman describes pipelined memory circuits as claimed.

In fact, though Lipman shows multiple tables that point to each other, nothing in Lipman's description teaches or suggests a lookup circuit comprising "M pipelined memory circuits" as claimed. The Examiner's statement that "these memory circuits are 'pipelined' in that they each point to another circuit" is not persuasive. Those of skill in the art recognize that a "pipeline" is a series of elements each connected so that the output of one element is an input of the next element. See, for example, Figure 3 of the present application, reproduced below, where the output of each pipelined SRAM is an input to the next one in series. Lipman does not appear to teach or suggest such a pipeline at all, much less pipelined memory circuits.

As illustrated above, Figure 3 of the instant application shows SRAM 321 is pipelined with 322, 323, 324, and 325, in that each memory circuit has an output connected to the input of the next memory circuit.

The Examiner refers to Lipman's Figure 7 for "pipelined memory circuits", but this figure shows a diagram of a data structure, not memory circuits. If the Examiner is intending to imply that the actual semiconductor circuits that comprise each bit/cell of a memory are the "memory circuits", then the Examiner will surely recognize that these are not typically pipelined, and Lipman certainly doesn't teach any such pipelining. Lipman doesn't teach series connections or pipelining of memory circuits at all.

The Examiner responds that “Lipman teaches pipelining via the levels of the ‘tree’ that are accessed in sequence. For example, a first tree level is accessed, followed by a second level, and third (i.e. a pipeline).” The Examiner’s response illustrates his misunderstanding. The sort of sequential access described by the Examiner is not a pipeline, as recognized by those of skill in the art. In a pipeline, data passes from a first element, directly to the next element, and then directly to the element after that. This is very different from, for example, a processor that sends data to/from a first element, then sends data to/from a second element, then sends data to/from a third element. A pipeline of elements is connected in series, not merely accessed in sequence.

The Examiner’s statement that “Pipelining is a term which is used to identify strings of several data or objects” is simply incorrect, particularly as applied to “strings of data”. The Examiner was requested to cite the source of this remarkable definition, but failed to do so.

In the Advisory Action, the Examiner makes the statement that “Pointers are used as simply [sic] representations of elements within circuits that are themselves inputs to another element.” Applicant respectfully notes that the Examiner may not fully understand the difference between a data structure and a physical hardware circuit – a pointer in a data structure normally has no relation at all to the underlying hardware, and nothing in Lipman suggests that it does so in this case.

This claim also requires an input-output processing (IOP) module coupled to the PMD modules and the switch fabric and capable of routing the data packets between the PMD modules and the switch fabric and between the PMD modules. This is not taught by Lipman.

The Examiner alleges that the IOP module is some combination of elements 188, 170, and 172. Nothing in Lipman indicates that small input buffer RAM 188, input FIFO 170, or output FIFO 172 are capable of routing the data packets between the PMD modules and the switch fabric and between the PMD modules, either individually or in combination.

This rejection should be reversed.

Claim 21

Independent claim 21 describes

A method for translating a first received address into a first destination address using M pipelined memory circuits that store a trie table, the method comprising the steps of:

accessing an address table in a first memory circuit using a first portion of the first received address;

outputting from the address table in the first memory circuit a first address pointer that indexes a start of an address table in a second memory circuit; and

accessing the address table in the second memory circuit using the first address pointer and a second portion of the first received address.

These limitations are similar to those discussed above with regard to Claims 1 and 11, and

those arguments are incorporated by reference.

Claim 21 also requires that the output from the address table in the first memory circuit is a first address pointer that indexes a start of an address table in a second memory circuit, similar to those limitations of Claims 2 and 12, and the arguments above with regard to those claims are incorporated by reference. These features are not taught or suggested by Lipman.

As described above, the output of the level-1 tree 150 (the NT pointer) is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). Lipman also describes that the base of the level-2 next tree table 152 is pointed to by the level 2 pointer 218 from the level pointer block 210. As such, it is clear that the NT pointer does not index a start of the address table in the second memory circuit, as claimed. As such, it is clear that Lipman also does not teach or suggest the features of independent claim 21. Claim 21 also requires M pipelined memory circuits, not taught or suggested by Lipman.

This rejection should be reversed.

Claim 22

These claims are dependent claims, and so the arguments above with respect to their respective parent claim(s) apply here as well, and are hereby incorporated by reference.

This claim requires outputting from address table in the second memory circuit a second address pointer that indexes a start of an address table in a third memory circuit; and accessing the address table in the third memory circuit using the second address pointer and a third portion of the

first received address. This is not taught by Lipman.

The elements referenced by the Examiner are not an output of a second memory circuit, where the second and third memory circuits are pipelined, as required by the parent claim. The entire rejection of this claim refers to Lipman's Figs. 12-14, which are flow diagrams for creating compressed trees, and have nothing at all to do with the claim limitations. Lipman does not discuss a process as claimed regarding accessing the address table in the third pipelined memory circuit using the second address pointer, from the second pipelined memory, and a third portion of the first received address.

These rejections should be reversed.

All rejections should be reversed.

Grouping of Claims

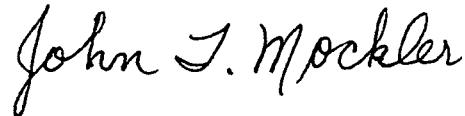
The claims on appeal do not stand or fall together, as may be seen from the arguments set forth below. Each claim or group of claims that has been argued separately under a separate subheading should be considered separately. While the applicant recognizes that a formal statement regarding the grouping of claims is no longer required, each claim should be considered separately; or at the very least each claim which is argued separately in the preceding sections of this brief should be considered separately.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance. The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: May 12, 2008

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DOCKET NO. 2003.09.014.BN0
Customer No. 23990

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : JACK C. WYBENGA, et al
Serial No. : 10/658,977
Filed : September 10, 2003
For : APPARATUS AND METHOD FOR PERFORMING HIGH-SPEED LOOKUPS IN A ROUTING TABLE
Group No. : 2189
Examiner : Reginald Glenwood Bragdon

APPENDIX A -

Claims Appendix

1. (Original) For use in a router, a lookup circuit for translating received addresses into destination addresses comprising:

M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

2. (Original) The lookup circuit as set forth in Claim 1, wherein said output of said first memory circuit comprises a first address pointer that indexes a start of said address table in said second memory circuit.

3. (Original) The lookup circuit as set forth in Claim 2, wherein said first address pointer and a second portion of said first received address access said address table in said second memory circuit.

4. (Original) The lookup circuit as set forth in Claim 3, wherein an output of said second memory circuit accesses an address table in a third memory circuit.

5. (Original) The lookup circuit as set forth in Claim 4, wherein said output of said second memory circuit comprises a second address pointer that indexes a start of said address table in said third memory circuit.

6. (Original) The lookup circuit as set forth in Claim 5, wherein said second address pointer and a third portion of said first received address access said address table in said third memory circuit.

7. (Original) The lookup circuit as set forth in Claim 6, wherein address pointers output from said M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, said routing table comprising a plurality of destination addresses associated with said received addresses.

8. (Original) The lookup circuit as set forth in Claim 7, further comprising a memory interface capable of selectively applying to said final memory circuit an address pointer associated with said first received address and an address pointer associated with a subsequently received address, such that said address pointer associated with said first received address is applied to said final memory circuit prior to said address pointer associated with said subsequently received address.

9. (Original) The lookup circuit as set forth in Claim 8, wherein said M pipelined memory circuits comprise static random access memory (SRAM) circuits.

10. (Original) The lookup circuit as set forth in Claim 9, wherein said final memory circuit comprises a dynamic random access memory (DRAM) circuit.

11. (Original) A router for interconnecting N interfacing peripheral devices, said router comprising:

a switch fabric; and

a plurality of routing nodes coupled to said switch fabric, each of said routing nodes comprising:

a plurality of physical medium device (PMD) modules capable of transmitting data packets to and receiving data packets from selected ones of said N interfacing peripheral devices;

an input-output processing (IOP) module coupled to said PMD modules and said switch fabric and capable of routing said data packets between said PMD modules and said switch fabric and between said PMD modules; and

a lookup circuit associated with said IOP module for translating received addresses associated with said data packets into destination addresses, said lookup circuit comprising M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

12. (Original) The router as set forth in Claim 11, wherein said output of said first memory circuit comprises a first address pointer that indexes a start of said address table in said second memory circuit.

13. (Original) The router as set forth in Claim 12, wherein said first address pointer and a second portion of said first received address access said address table in said second memory circuit.

14. (Original) The router as set forth in Claim 13, wherein an output of said second memory circuit accesses an address table in a third memory circuit.

15. (Original) The router as set forth in Claim 14, wherein said output of said second memory circuit comprises a second address pointer that indexes a start of said address table in said third memory circuit.

16. (Original) The router as set forth in Claim 15, wherein said second address pointer and a third portion of said first received address access said address table in said third memory circuit.

17. (Original) The router as set forth in Claim 16, wherein address pointers output from said M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, said routing table comprising a plurality of destination addresses associated with said received addresses.

18. (Original) The router as set forth in Claim 17, further comprising a memory interface capable of selectively applying to said final memory circuit an address pointer associated with said first received address and an address pointer associated with a subsequently received address, such that said address pointer associated with said first received address is applied to said final memory circuit prior to said address pointer associated with said subsequently received address.

19. (Original) The router as set forth in Claim 18, wherein said M pipelined memory circuits comprise static random access memory (SRAM) circuits.

20. (Original) The router as set forth in Claim 19, wherein said final memory circuit comprises a dynamic random access memory (DRAM) circuit.

21. (Original) A method for translating a first received address into a first destination address using M pipelined memory circuits that store a trie table, the method comprising the steps of:

accessing an address table in a first memory circuit using a first portion of the first received address;

outputting from the address table in the first memory circuit a first address pointer that indexes a start of an address table in a second memory circuit; and

accessing the address table in the second memory circuit using the first address pointer and a second portion of the first received address.

22. (Original) The method as set forth in Claim 21 further comprising the steps of:

outputting from address table in the second memory circuit a second address pointer that indexes a start of an address table in a third memory circuit; and

accessing the address table in the third memory circuit using the second address pointer and a third portion of the first received address.



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Filed : September 10, 2003
For : APPARATUS AND METHOD FOR PERFORMING HIGH-SPEED LOOKUPS IN A ROUTING TABLE
Group No. : 2189
Examiner : Reginald Glenwood Bragdon

APPENDIX B -
Copy of Formal Drawings

Appeal Brief – Serial No. 10/658,977.....Appendix B

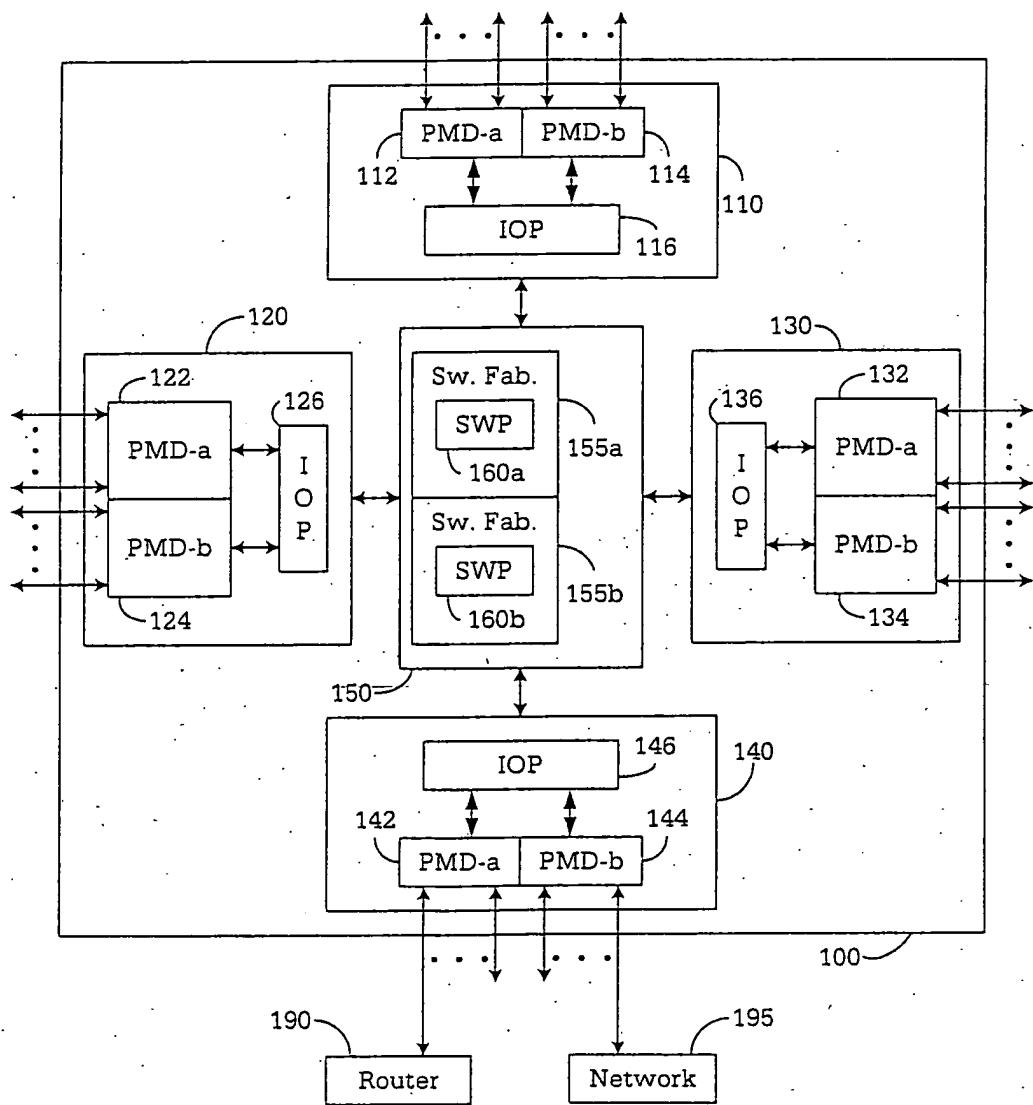


FIGURE 1

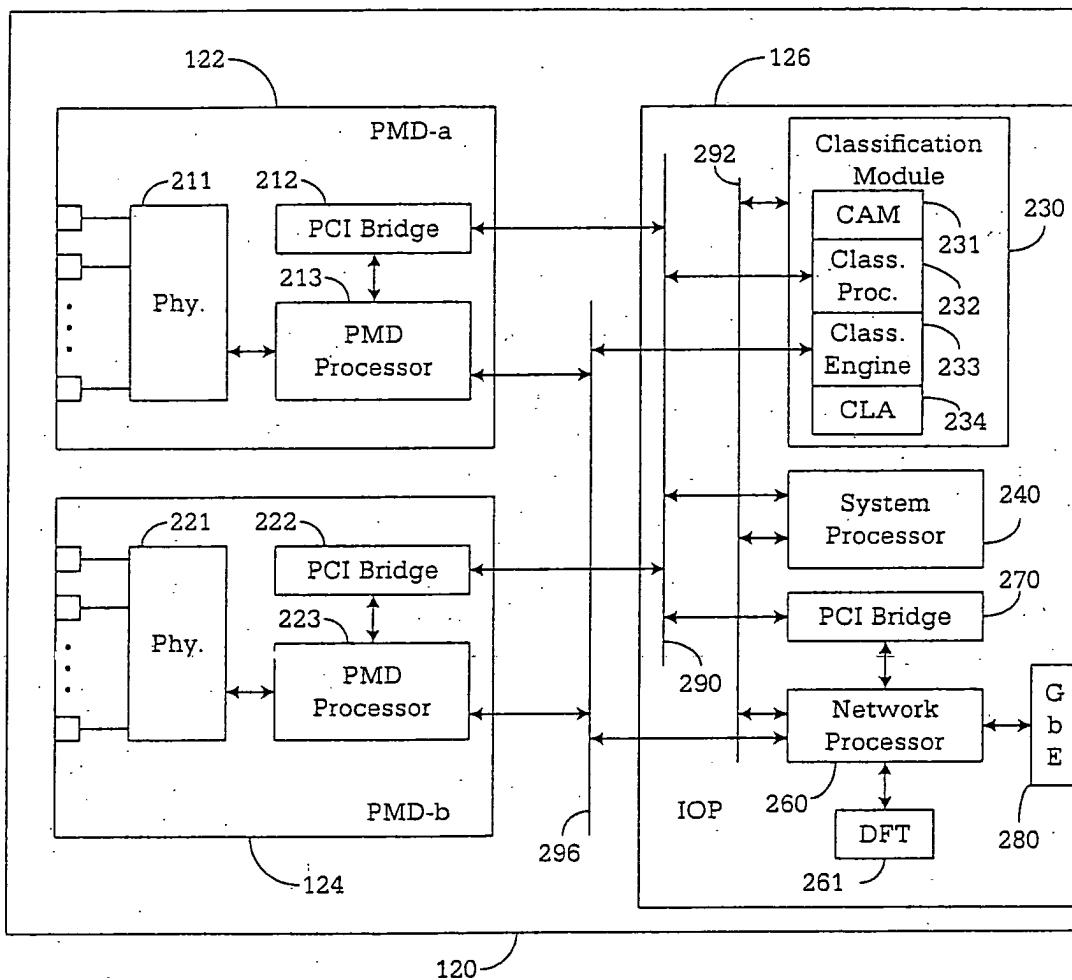


FIGURE 2

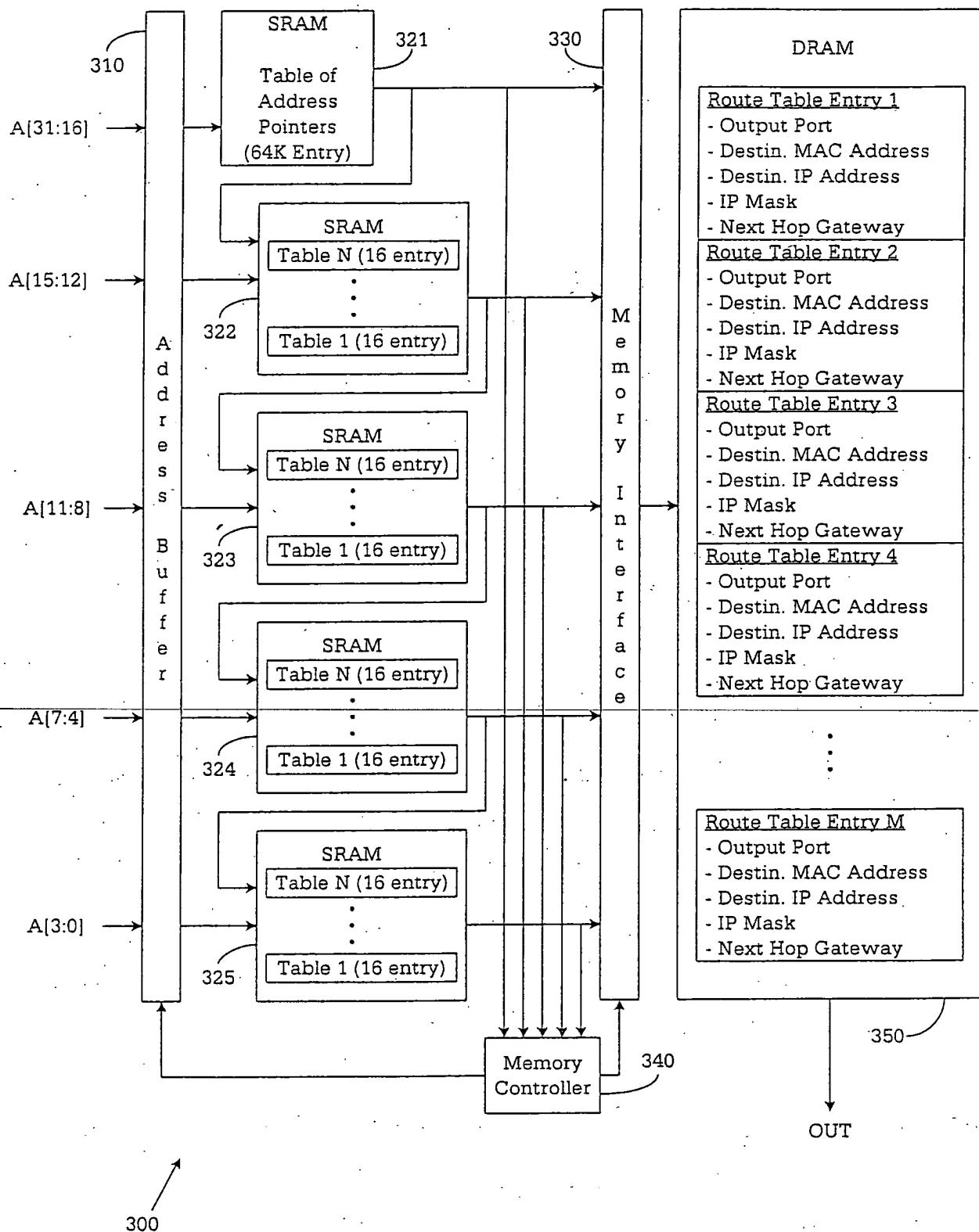


FIGURE 3

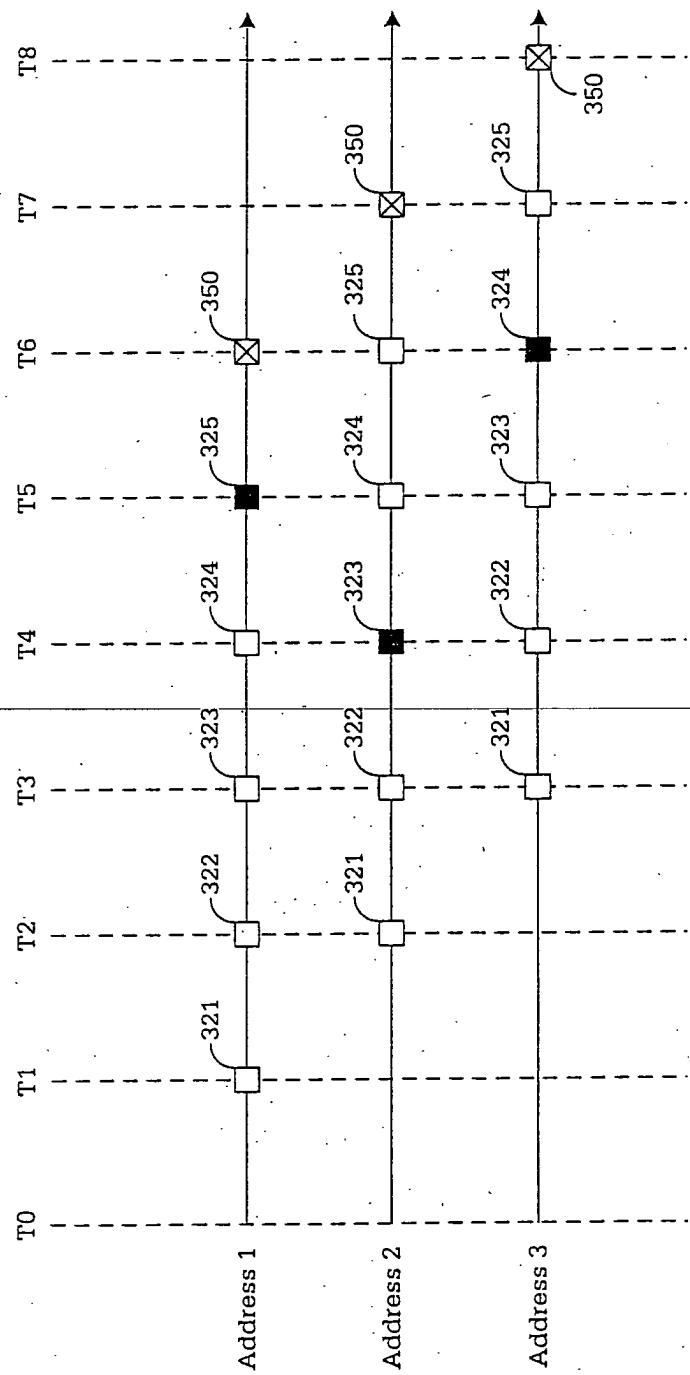
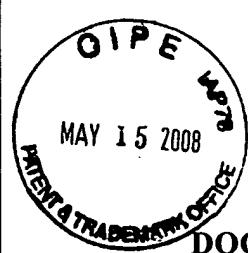


FIGURE 4



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APPENDIX C -
Evidence Appendix

Not Applicable -- No other evidence was entered.

Appeal Brief – Serial No. 10/658,977.....*Appendix C*



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APPENDIX D -
Related Proceedings Appendix

Not Applicable -- To the best knowledge and belief of the undersigned attorney, there are none.

Appeal Brief – Serial No. 10/658,977.....Appendix D